REMARKS

These comments are responsive to the non-final Office Action dated August 10, 2007. The Office Action rejected claims 1-17, 35 and 37-42 under 35 U.S.C. § 103(a) as being unpatentable over Conley (US2002/0099904) in view of Chien et al. (US patent number 6,742,078).

With respect to claims 35 and 37-42, these were all originally dependent upon claim 28 as their base claim. Claims 28-34 were cancelled in response to the previous Office Action due to the nature of the rejection, as described in the previous Amendment in response to this Office Action. Given the new grounds of the current rejection, which is argued below, the reasons for which these claims were cancelled are no longer present; however, rather than to bring back these claims at this time, claims 35 and 37-42 will be cancelled at this time and will likely be pursued together as claims 28-42 in continuation at a later time.

With respect to claims 1-17, although it is believed that the Office Action's rejection of claim 1 is not well founded for reasons given below, claim 1 has now been cancelled and claims 4, 10, and 11 rewritten in independent form to further delineate the distinctions from the prior art. The other remaining claims have one of either claim 4, 10, or 11 as base claim.

Claim 4

Claim 4 includes the elements of:

> establishing a set of metablock linkings, each comprised of a plurality of units of erase, by which the controller accesses the non-volatile memory;

for which the Office Action cites Conley and

> storing a record of said metablock linkings in the non-volatile memory;

for which the Office Action cites Chien. Claim 4 has been rewritten in independent form by incorporating these elements from claim 1. In its rejection of claim 1, the Office Action states that it would be obvious to take a metablock linking, such as Conley presents, and, based on the teachings of Chien, store a record of this linking in the non-volatile memory as described by these elements. It is respectfully submitted that this basis of rejection is not well founded.

Chien presents a "link-table block" that is in the flash memory and that "is used to record the link relationship between the logic address and the actual address", as described there at column 4, lines 34-37. However, as described in the locations cited in the office action, this

linking is just a basic logical to physical translation between logical memory blocks and physical memory blocks. There is no disclosure or suggestion of how the described mechanisms could be extended to the sort of metablock structure presented by Conley, which links together multiple *physical* blocks from differing sub-arrays. Rather than storing a logical-to-physical conversion, this would require storing of a record of which of these differing physical blocks have been linked together as a composite structure. Instead, Chien relies on the sort of FAT link table described there with respect to Figure 11 that records which individual physical block corresponds to a respective logical block. It is neither taught nor suggested how this structure could be used to include the linking of multiple physical blocks in the composite metablock structure.

Claim 4 is believed further allowable based on its additional elements. The next elements of claim 4,

> determining that a unit of erase in a first of said metablock linkings is defective;
> updating the first metablock linking so that it no longer contains said defective unit of erase;

for which the Office Action cites Chien at column 3, lines 43-46, and column 3, line 63, to column 4, line 20. It is important to note that these elements describe the re-linking of the blocks (units of erase) *within* the composite metablock, rather than the linking of a single logical block to a single physical block. (For instance, if a metablock linking included physical block A in sub-array 1, block B in sub-array 2, block C in sub-array 3, and block D in sub-array 4, this would correspond to determining that block C, say, is defective and replacing it with another block, say C', so that the metablock is now formed of the physical blocks A, B, C', and D.) Chien neither teaches nor suggests the use of metablocks, much less the idea of updating such a linking. Rather, the cited locations in Chien disclose the re-linking of a single logical block to a single physical block.

Therefore, for at least these reasons, it is respectfully submitted that a rejection of claim 4 under U.S.C. § 103(a) as being unpatentable over Conley in view of Chien is not well founded and that claim 4, along with its dependent claims (claims 2, 3, 5-9, and 12-17), are allowable. A number of these dependent claims include further limitation that are believed to make them further allowable; however, given the basic differences between what is presented in independent claim 4 and what is found in the cited references, these will not discussed at present.

Claims 10 and 11

Claims 10 and 11 are also rejected under U.S.C. § 103(a) as being unpatentable over Conley in view of Chien. Both claims 10 and 11 have rewritten in independent form by incorporating the elements of claim 1. Consequently, as discussed above with respect to claim 4, both are believed allowable due to the elements of:

> establishing a set of metablock linkings, each comprised of a plurality of units of erase, by which the controller accesses the non-volatile memory;
> storing a record of said metablock linkings in the non-volatile memory;

as discussed above with respect to claim 4.

Additionally, claim 10 includes the elements of:

> maintaining a list of unlinked units of erase;
> determining that one or more units of erase in a first of said metablock linkings is defective; and
> adding the non-defective units of erase in the first metablock to the list of unlinked units of erase.

for which the Office Action cites Chien's Figure 4, at column 3, line 65, to column 4, line 20, and at column 5, lines 18-30. These elements describe a process of determining that a metablock linking includes one or more defective blocks and then adding the non-defective blocks from the metablock to a list of blocks that are not linked into metablocks; that is, it describes a process where, when a metablock is determined to include a defective block, the metablock is broken down and its good blocks are returned to the pool of unlinked blocks. Chien neither teaches nor suggests the use of metablocks, much less the idea of breaking down such a linking and returning its good blocks back to a pool of unlinked blocks. Rather, the cited locations in Chien disclose the remapping of a logical block from a defective physical block to a good physical block.

Concerning claim 11, this includes the elements of:

> determining that a unit of erase in a first of said metablock linkings is defective;
> determining whether an alternate unit of erase is available for the defective unit of erase; and
> in response to determining that an alternate unit of erase is not available, removing the first metablock from the set of metablock linkings.

These elements describe a process of determining that a metablock linking includes a defective blocks, looking for a replacement, and, if not, retiring the metablock from the list of linked metablocks. Chien neither teaches nor suggests the use of metablocks, much less the idea of looking for a replacement block for a defective block in the metablock linking and then unlinking the block if no replacement is available. Rather, the cited locations in Chien again just

disclose the remapping of a logical block from a defective physical block to a good physical block.

Therefore, for at least these reasons, it is respectfully submitted that a rejection of claims 10 and 11 under U.S.C. § 103(a) as being unpatentable over Conley in view of Chien is not well founded.

Conclusion

Consequently, it is now believed that the present application is now in form for allowance, an early indication of which is earnestly solicited.

Respectfully submitted,

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